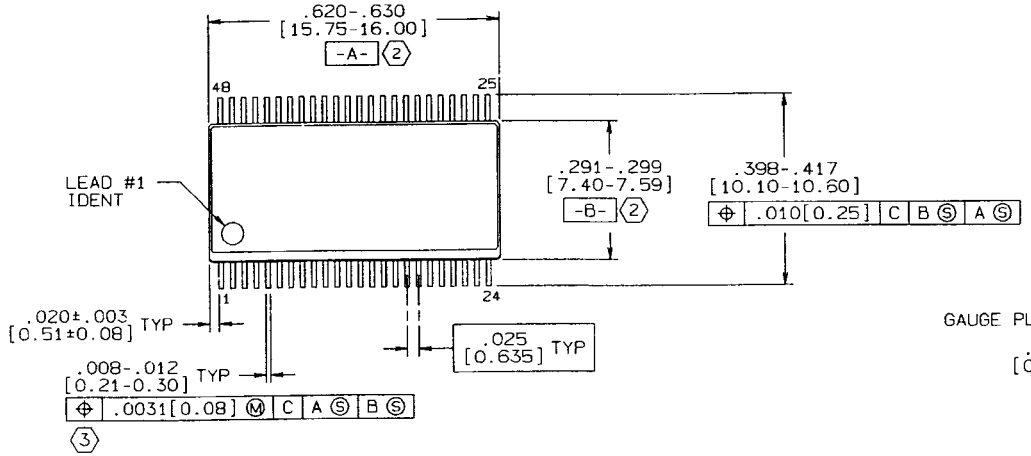
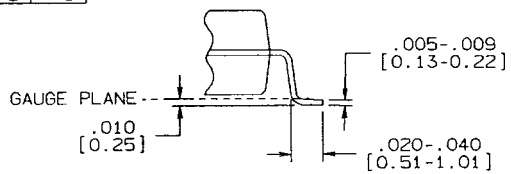
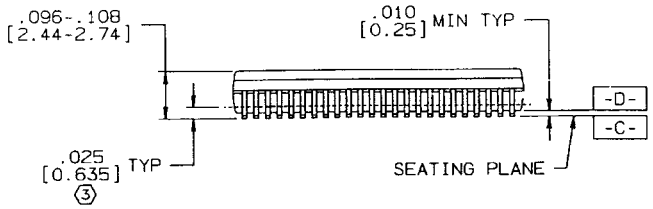
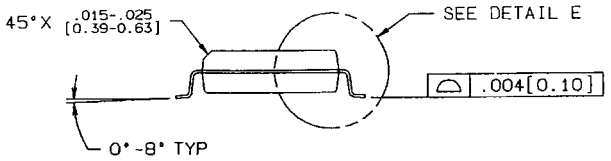
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	08420	04/01/91	DEG/CC
B	ADD NOTE 4; LD TRUE POS TOL WAS .010	10169	03/15/94	TL/CC
C	TRUE POS: .0063[0.16] WAS .007[0.18]; LD PITCH: [0.635] WAS [0.63]; STANDOFF: .010[0.25] MIN WAS .008-.016 [0.21-0.40]; LD TIP TO LD TIP: .398-.417[10.11-10.59] WAS .395-.420[10.04-10.66].	10495	07/19/94	MS/DM
D	⌖ .0031[0.08] Ⓜ C A Ⓢ B Ⓢ WAS ⌖ .0063[0.160] Ⓜ D A Ⓢ B Ⓢ	10604	09/26/94	MS/KHT
E	TOP VIEW: ADD DIM .020±.003[0.51±0.08]; CHANGE DWG SIZE FROM B TO C.	11229	11/01/95	MS/ES





DETAIL E TYP





CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   200 MICROINCHES/5.08 MICROMETERS MINIMUM LEAD/TIN (SOLDER) ON COPPER.
2. (2) DIMENSION DOES NOT INCLUDE MOLD FLASH.
3. (3) MAXIMUM LEAD WIDTH ABOVE AREA SPECIFIED .018[0.45].
4. REFERENCE JEDEC REGISTRATION MO-118, VARIATION AA, DATED JUNE 1993.

APPROVALS	DATE
DRAWN D.E.GRADY	04/01/91
DES. CHK.	11/6/95
ENGR. CHK.	11/03/95

PROJECTION INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

MOLDED PACKAGE, SSOP, .300 WIDE, 48 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-MS48A	E

DO NOT SCALE DRAWING | SHEET 1 OF 1